

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 11-18, without prejudice.

1. (ORIGINAL) A semiconductor package obtained by collectively fabricating a plurality of semiconductor packages on a wafer in a batch process and dicing the resulting wafer product into discrete semiconductor packages, wherein

said semiconductor package is a stacked body formed by bonding two or more semiconductor devices through an insulating layer;

each of said semiconductor devices comprises a substrate and a device pattern formed on a surface thereof; and

a device pattern surface of a lower semiconductor device faces a non-device pattern surface of a semiconductor device stacked on said lower semiconductor device.

2. (ORIGINAL) A semiconductor package as defined in claim 1, wherein said semiconductor device positioned as the lowermost layer further comprises a heat radiation layer, formed of a material having a high heat transfer rate, on the non-device pattern surface thereof.

3. (ORIGINAL) A semiconductor package as defined in claim 2, wherein said heat radiation layer is one deposited on the non-device pattern surface of a wafer as the lowermost layer, before said semiconductor packages are diced.

4. (PREVIOUSLY PRESENTED) A semiconductor package as defined in claim 2, wherein said heat radiation layer is one formed by a thin film formation technology.

5. (PREVIOUSLY PRESENTED) A semiconductor package as defined in claim 2, wherein said heat radiation layer is made of copper, aluminum or an alloy.

6. (PREVIOUSLY PRESENTED) A semiconductor package as defined in claim 2, wherein said heat radiation layer also acts as a support.

7. (PREVIOUSLY PRESENTED) A semiconductor package as defined in claim 1, wherein said insulating layer comprises a polyimide resin or an epoxy resin.

8. (PREVIOUSLY PRESENTED) A semiconductor package as defined in claim 1, wherein said semiconductor device positioned as the uppermost layer further comprises a resin sealing layer on the device pattern surface thereof, and said resin sealing layer is one formed on the device pattern surface of the wafer as the uppermost layer, before said semiconductor package is diced.

9. (PREVIOUSLY PRESENTED) A semiconductor package as defined in claim 1, wherein the device patterns of said semiconductor devices stacked are electrically connected to one another through a re-wiring layer and a substrate through-electrode that are simultaneously formed in one semiconductor device.

10. (ORIGINAL) A semiconductor package as defined in claim 9, wherein each of said re-wiring layer and said substrate through-electrode is formed of copper or its alloy.

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